IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:)
MARIAUD ET AL.)
Serial No. **Not Yet Assigned**)
)
Filing Date: **Herewith**)
)
For: **DEVICE FOR AUTOMATICALLY CONTROLLING A VOLTAGE APPLIED TO A DATA CONDUCTOR IN A SERIAL LINK**)

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EXPRESS MAIL NO: EL747059657US

DATE OF DEPOSIT: November 16, 2001

NAME: Greg Freyer

SIGNATURE:

PRELIMINARY AMENDMENT

Director, U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Prior to the calculation of fees and examination of the present application, please enter the amendments and remarks set out below.

In the Drawings:

Submitted herewith is a request for proposed drawing modifications as indicated in red ink to label FIGS. 1-3 as prior art. The functional blocks in FIGS. 1 and 6 are being labeled as indicated in red ink, and FIG. 3 is being modified as indicated in red ink to correct a misspelled word. FIG. 4 is also being modified to translate reference labels as indicated in red ink.

In the Claims:

Please cancel Claims 1 to 6.

Please add new Claims 7 to 26.

7. A control device for controlling a first voltage applied to a first conductor wire of a universal serial bus (USB) in a first peripheral apparatus connected upstream to a second peripheral apparatus, the first peripheral apparatus comprising a supply voltage source for supplying the first voltage to the first conductor wire and for receiving on a second conductor wire of the USB a second voltage, the control device comprising:

a detection circuit connected to the second conductor wire of the USB for detecting the second voltage received therefrom;

a memory connected to said detection circuit for storing a logic value corresponding to a presence or an absence of the second voltage; and

a logic control circuit connected to said memory for operating the supply voltage source only if the second voltage is present.

8. A control device according to Claim 7, wherein said detection circuit comprises:

a Schmitt trigger having an input connected to the second conductor wire of the USB, and an output for providing an output signal;

an edge detection circuit connected to an output of said Schmitt trigger for detecting a rising edge or a falling edge of the output signal, and for producing at least one signal corresponding to the detected rising and falling edges of the output signal;

a counter connected to said edge detection circuit

for counting a duration from which a logic value of the detected rising edge or of the detected falling edge of the output signal is maintained, and for producing an end of count signal when the counted duration reaches a predetermined value; and

a state machine connected between said edge detector and said counter for changing logic states as a function of the detected rising edge and the detected falling edge of the output signal and as a function of the end of count signal, said state machine producing a signal having a logic value corresponding to the presence or absence of the second voltage and for producing a signal indicating that the logic value corresponding to the presence or absence of the second voltage has changed.

9. A control device according to Claim 7, further comprising a state register comprising at least one latch; and wherein said memory circuit comprises said at least one latch.

10. A control device according to Claim 7, wherein said logic control circuit comprises:

an inverter circuit having an input terminal for receiving the logic value corresponding to the presence or absence of the second voltage; and

a NOR circuit having a first input connected to an output terminal of said inverter circuit, and a second input for receiving a logic value indicating that the supply voltage source can be operated.

11. A control device according to Claim 7, wherein the first peripheral apparatus comprises a microcontroller, an

interrupt state register (ISR) for the microcontroller and comprising a plurality of latches, and an interrupt mask register (IMR) for the microcontroller and comprising a plurality of latches; the control device further comprising:

a circuit for interrupting the microcontroller and comprising

at least one latch from the ISR for recording a change in the logic value corresponding to the presence or absence of the second voltage,

at least one latch from the IMR for recording whether the microcontroller requires knowledge of the logic value recorded in said at least one latch from the ISR, and

an AND circuit having a first input connected to said at least one latch from the ISR and a second input connected to said at least one latch from the IMR, and an output for providing an interrupt request signal to the microcontroller only if there occurs a change in the logic value corresponding to the presence or absence of the second voltage and if the logic value recorded in said at least one latch from the ISR has a 1 logic value.

12. A control device according to Claim 7, wherein the first conductor wire in the USB comprises a data conductor wire.

13. A first peripheral apparatus connected upstream to a second peripheral apparatus via a universal serial bus (USB), the first peripheral apparatus comprising:

a supply voltage source connected to a first

conductor wire in the USB for supplying a first voltage thereto;

a detection circuit connected to a second conductor wire of the USB for detecting a second voltage received therefrom;

a memory connected to said detection circuit for storing a logic value corresponding to a presence or an absence of the second voltage; and

a logic control circuit connected to said memory for operating said supply voltage source only if the second voltage is present.

14. A first peripheral apparatus according to Claim 13, wherein said detection circuit comprises:

a Schmitt trigger having an input connected to the second conductor wire of the USB, and an output for providing an output signal;

a edge detection circuit connected to an output of said Schmitt trigger for detecting a rising edge or a falling edge of the output signal, and for producing at least one signal corresponding to the detected rising and falling edges of the output signal;

a counter connected to said edge detection circuit for counting a duration from which a logic value of the detected rising edge or of the detected falling edge of the output signal is maintained, and for producing an end of count signal when the counted duration reaches a predetermined value; and

a state machine connected between said edge detector and said counter for changing logic states as a function of the detected rising edge and the detected falling edge of the

output signal and as a function of the end of count signal, said state machine producing a signal having a logic value corresponding to the presence or absence of the second voltage and for producing a signal indicating that the logic value corresponding to the presence or absence of the second voltage has changed.

15. A first peripheral apparatus according to Claim 13, further comprising a state register comprising at least one latch; and wherein said memory circuit comprises said at least one latch.

16. A first peripheral apparatus according to Claim 13, wherein said logic control circuit comprises:

an inverter circuit having an input terminal for receiving the logic value corresponding to the presence or absence of the second voltage; and

a NOR circuit having a first input connected to an output terminal of said inverter circuit, and a second input for receiving a logic value indicating that said supply voltage source can be operated.

17. A first peripheral apparatus according to Claim 13, further comprising:

a microcontroller;

an interrupt state register (ISR) for said microcontroller and comprising a plurality of latches;

an interrupt mask register (IMR) for said microcontroller and comprising a plurality of latches; and

a circuit for interrupting said microcontroller and comprising

at least one latch from said ISR for recording a change in the logic value corresponding to the presence or absence of the second voltage,

at least one latch from said IMR for recording whether said microcontroller requires knowledge of the logic value recorded in said at least one latch from said ISR, and

an AND circuit having a first input connected to said at least one latch from said ISR and a second input connected to said at least one latch from said IMR, and an output for providing an interrupt request signal to said microcontroller only if there occurs a change in the logic value corresponding to the presence or absence of the second voltage and if the logic value recorded in said at least one latch from said ISR has a 1 logic value.

18. A first peripheral apparatus connected upstream to a second peripheral apparatus via a universal serial bus (USB), the first peripheral apparatus comprising:

a supply voltage source connected to a first conductor wire in the USB for supplying a first voltage thereto;

a detection circuit connected to a second conductor wire of the USB for detecting a second voltage received therefrom;

a memory connected to said detection circuit for storing a logic value corresponding to a presence or an absence of the second voltage; and

a logic control circuit connected to said memory for

operating said supply voltage source only if the second voltage is present, said logic control circuit comprising

an inverter circuit having an input terminal connected to said memory for receiving the logic value corresponding to the presence or absence of the second supply voltage stored, and

a NOR circuit having a first input connected to an output terminal of said inverter circuit, and a second input for receiving a logic value indicating that said supply voltage source can be operated.

19. A first peripheral apparatus according to Claim 18, wherein said detection circuit comprises:

a Schmitt trigger having an input connected to the second conductor wire of the USB, and an output for providing an output signal;

a edge detection circuit connected to an output of said Schmitt trigger for detecting a rising edge or a falling edge of the output signal, and for producing at least one signal corresponding to the detected rising and falling edges of the output signal;

a counter connected to said edge detection circuit for counting a duration from which a logic value of the detected rising edge or of the detected falling edge of the output signal is maintained, and for producing an end of count signal when the counted duration reaches a predetermined value; and

a state machine connected between said edge detector and said counter for changing logic states as a function of the detected rising edge and the detected falling edge of the output signal and as a function of the end of count signal,

said state machine producing a signal having a logic value corresponding to the presence or absence of the second voltage and for producing a signal indicating that the logic value corresponding to the presence or absence of the second voltage has changed.

20. A first peripheral apparatus according to Claim 18, further comprising a state register comprising at least one latch; and wherein said memory circuit comprises said at least one latch.

21. A first peripheral apparatus according to Claim 18, further comprising:

a microcontroller;

an interrupt state register (ISR) for said microcontroller and comprising a plurality of latches;

an interrupt mask register (IMR) for said microcontroller and comprising a plurality of latches; and

a circuit for interrupting said microcontroller and comprising

at least one latch from said ISR for recording a change in the logic value corresponding to the presence or absence of the second voltage,

at least one latch from said IMR for recording whether said microcontroller requires knowledge of the logic value recorded in said at least one latch from said ISR, and

an AND circuit having a first input connected to said at least one latch from said ISR and a second input connected to said at least one latch from said IMR, and an output for providing an

interrupt request signal to said microcontroller only if there occurs a change in the logic value corresponding to the presence or absence of the second voltage and if the logic value recorded in said at least one latch from said ISR has a 1 logic value.

22. A method for automatically controlling a first voltage being applied to a first conductor wire of a universal serial bus (USB) in a first peripheral apparatus connected upstream to a second peripheral apparatus, the first peripheral apparatus comprising a supply voltage source for supplying the first voltage to the first conductor wire and receives on a second conductor wire of the USB a second voltage, the method comprising:

detecting in the first peripheral apparatus the second voltage received on the second conductor wire of the USB;

storing in the first peripheral apparatus a logic value corresponding to a presence or an absence of the second voltage; and

operating the supply voltage source only if the second voltage is present based upon a comparison with the stored logic value using a logic circuit.

23. A method according to Claim 22, wherein the detecting comprises:

generating an output signal from a Schmitt trigger having an input connected to the second conductor wire of the USB;

detecting a rising edge or a falling edge of the

output signal, and producing at least one signal corresponding to the detected rising and falling edges of the output signal;

counting a duration from which a logic value of the detected rising edge or of the detected falling edge of the output signal is maintained, and for producing an end of count signal when the counted duration reaches a predetermined value; and

using a state machine for changing logic states as a function of the detected rising edge and the detected falling edge of the output signal and as a function of the end of count signal, the state machine for producing a signal having a logic value corresponding to the presence or absence of the second voltage and for producing a signal indicating that the logic value corresponding to the presence or absence of the second voltage has changed.

24. A method according to Claim 22, wherein the first peripheral apparatus comprises a state register comprising at least one latch; and wherein the logic value corresponding to the presence or absence of the second voltage is stored in the at least one latch.

25. A method according to Claim 22, wherein operating the supply voltage source comprises:

inverting the logic value corresponding to the presence or absence of the second voltage; and

using a NOR circuit having a first input for receiving the inverted logic value corresponding to the presence or absence of the second voltage, and a second input for receiving a logic value indicating that the supply voltage source can be operated.

26. A method according to Claim 22, wherein the first peripheral apparatus comprises a microcontroller, an interrupt state register (ISR) for the microcontroller and comprising a plurality of latches, and an interrupt mask register (IMR) for the microcontroller and comprising a plurality of latches; and wherein the method further comprises:

interrupting the microcontroller by

recording in the at least one latch from the ISR a change in the logic value corresponding to the presence or absence of the second voltage,

recording in the at least one latch from the IMR whether the microcontroller requires knowledge of the logic value recorded in the at least one latch from the ISR, and

using an AND circuit having a first input connected to the at least one latch from the ISR and a second input connected to the at least one latch from the IMR, for providing at an output an interrupt request signal to the microcontroller only if there occurs a change in the logic value corresponding to the presence or absence of the second voltage and if the logic value recorded in the at least one latch from the ISR has a 1 logic value.

REMARKS

It is believed that all of the claims are patentable over the prior art. For better readability and the Examiner's convenience, the newly submitted claims differ from the translated counterpart claims which are being canceled. The

newly submitted claims do not represent changes or amendments that narrow the claim scope for any reason related to the statutory requirements for patentability. Accordingly, after the Examiner completes a thorough examination and finds the claims patentable, a Notice of Allowance is respectfully requested in due course. Should the Examiner determine any minor informalities that need to be addressed, he is encouraged to contact the undersigned attorney at the telephone number below.

Respectfully submitted,

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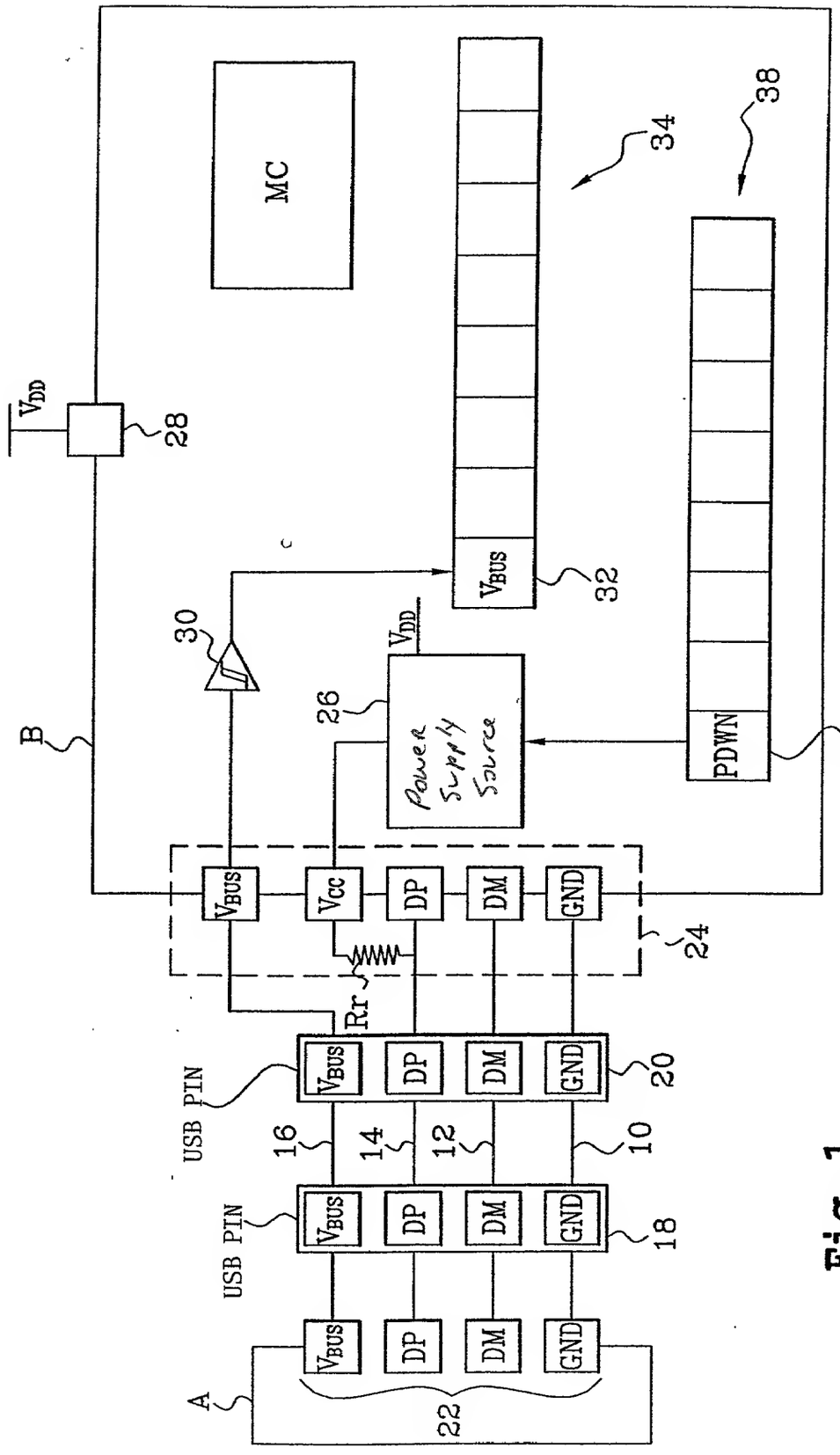


Fig. 1
(PRIOR ART)

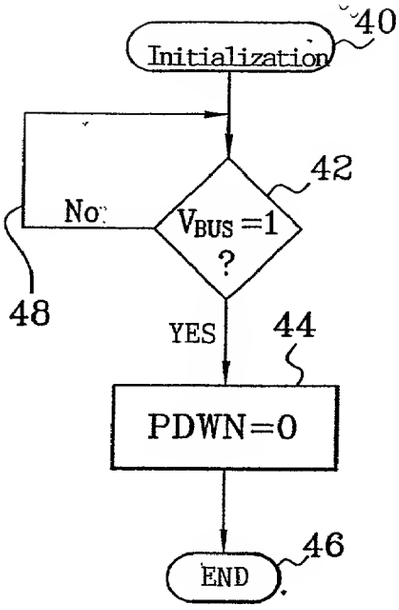


Fig. 2
(PRIOR ART)

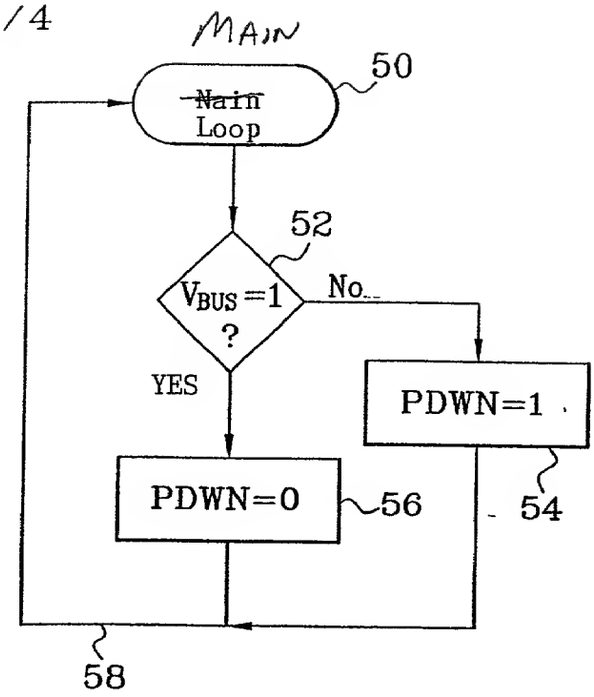


Fig. 3
(PRIOR ART)

Fig. 4

VBUSSTAT	PDWN	State of Regulator 26
0	0	~~Arrêt~~ Stop
0	1	~~Arrêt~~ Stop
1	0	~~Marche/Walk~~ Go
1	1	~~Arrêt~~ Stop

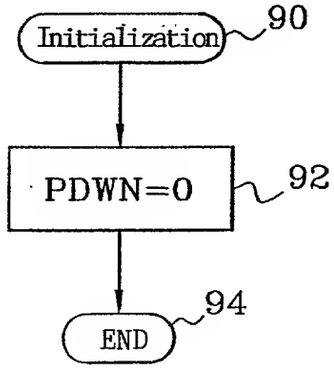


Fig. 5

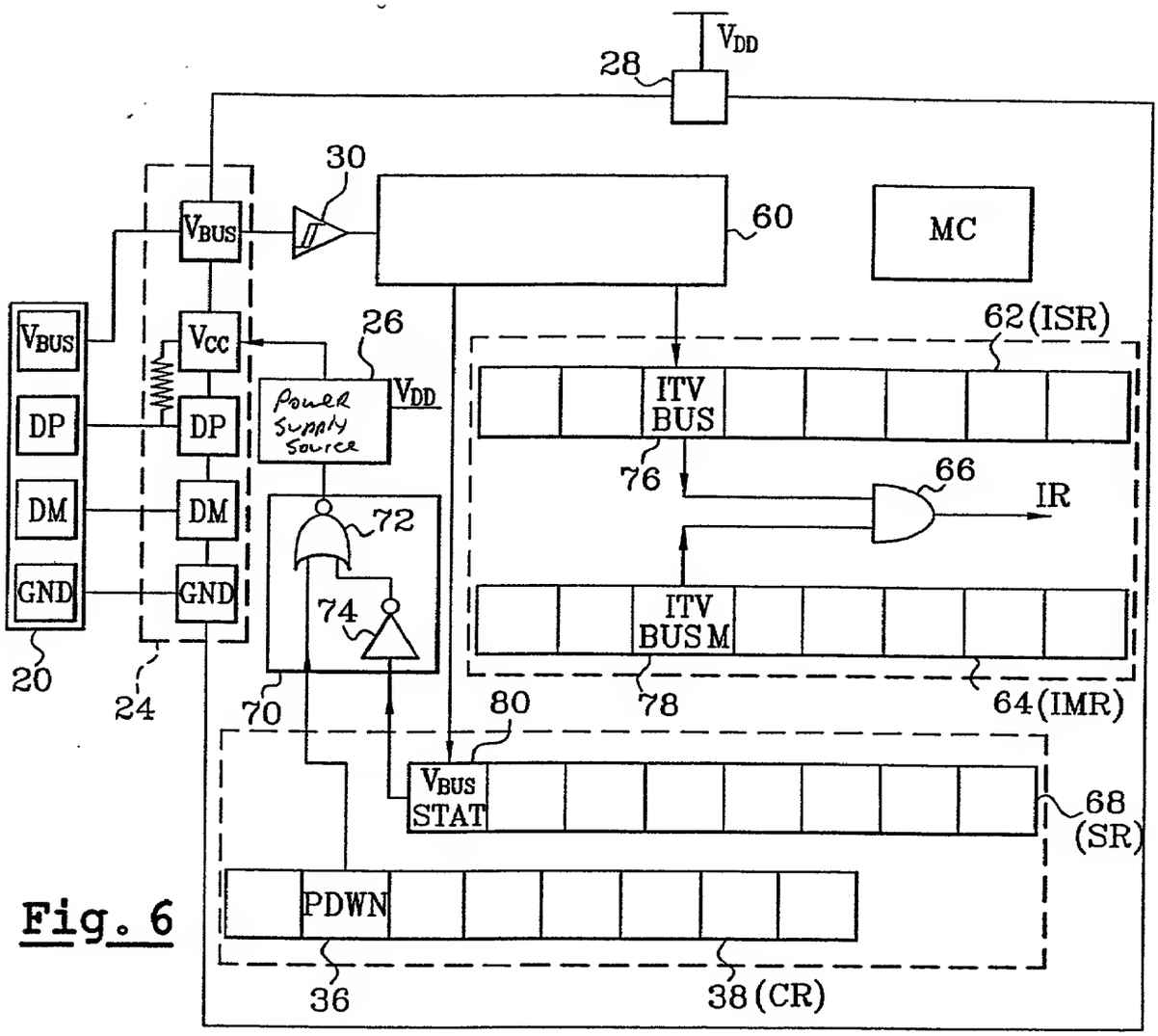
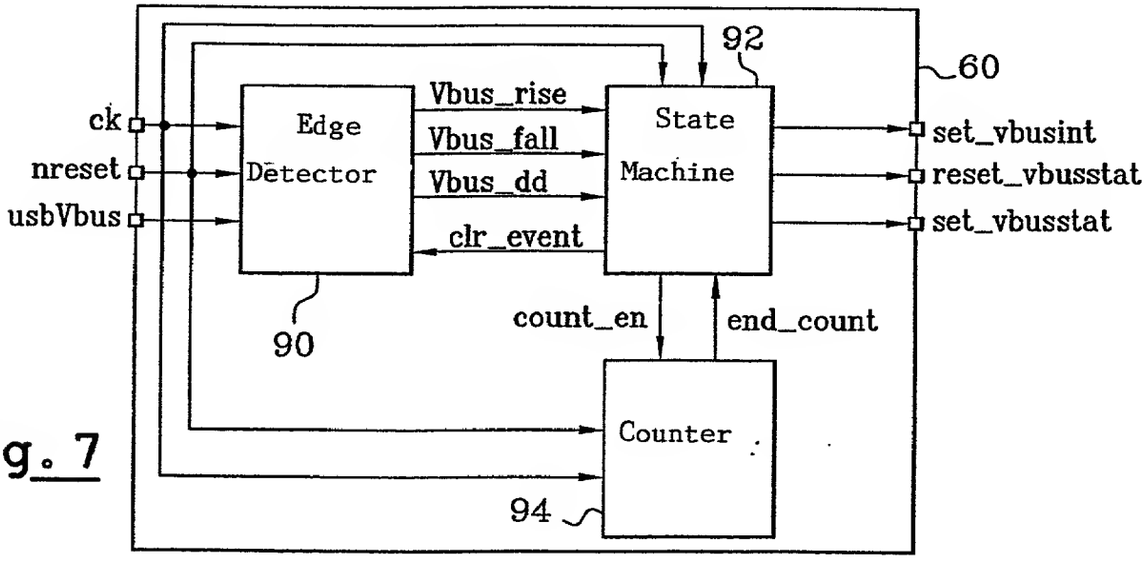

VDD
28
30
60
MC
VBUS
Vcc
DP
DM
GND
26
Power Supply Source
VDD
62(ISR)
ITV BUS
76
66
IR
72
74
ITV BUS M
20
24
70
80
78
64(IMR)
VBUS STAT
68 (SR)
PDWN
36
38(CR)

Fig. 6


92
60
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Edge Detector
Vbus_rise
Vbus_fall
Vbus_dd
clr_event
State Machine
set_vbusint
reset_vbusstat
set_vbusstat
90
count_en
end_count
Counter
94

Fig. 7